What is claimed is :

1. An apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a plurality of performance monitor means, connected respectively to bus lines which are connected with devices mounted on said motherboard, for monitoring the operating state of each said device according to the flow rate of data transferred in said bus lines; and

a performance control chip, connected separately to said devices, for adjusting the operating rate of said devices responsive to said performance monitor means, said performance control chip being capable of ascertaining the operating state of each said device is busy or not, so as to increasing or decreasing the operating rate of said device.

2. The apparatus according to Claim 1, wherein said bus lines comprise:

a PCI bus line, connected between a south bridge chip and a PCI slot;

an AGP bus line, connected between a north bridge chip and an AGP slot;

a RAM bus line, connected between said north bridge chip and a RAM device; and

a CPU bus line, connected between a CPU and said north bridge chip.

3. The apparatus according to Claim 1, wherein said devices

connected to said performance control chip comprise a CPU, a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

4. The apparatus according to Claim 1, wherein said performance monitor means comprises a counter, for measuring the number of times of transferring commands or accessing data through one selected said bus line per unit time.

5. The apparatus according to Claim 1, wherein said performance control chip comprises:

a register, for storing predetermined flow rates of said devices;

a comparator, for comparing actual flow rates provided by said performance monitor means with said predetermined flow rates stored in said register, when said actual flow rate of one selected said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy.

6. The apparatus according to Claim 1, wherein said performance control chip is connected to a motherboard power supply on said motherboard and is capable of controlling said operating rate of each said device by adjusting the power supplied thereto.

7. An apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a plurality of counters, coupled respectively to the corresponding one of bus lines which are connected with devices, for measuring the flow rate of data transferred in each said bus line per unit time; and

a performance control chip, connected separately to said devices, being capable of ascertaining each said device is busy or not, so as to increasing or decreasing the operating rate of said device, said performance control chip comprising

a register, for storing predetermined flow rates of said devices;

a comparator, for comparing actual flow rates measured by said counter with said predetermined flow rate stored in said register, when said actual flow rate of one said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy.

8. The apparatus according to Claim 7, wherein said bus lines comprise:

a PCI bus line, connected between a south bridge chip and a PCI slot;

an AGP bus line, connected between a north bridge chip and an AGP slot;

a RAM bus line, connected between said north bridge chip and a RAM device; and

a CPU bus line, connected between a CPU and said north bridge chip.

9. The apparatus according to Claim 7, wherein said devices

connected to said performance control chip comprise a CPU, a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

10. A method for adjusting the system performance of a computer, for monitoring the actual data flow rates of devices fabricated on a motherboard and adjusting the operating rates of said devices, said method comprising the steps of:

(1) executing a program to make one selected said device be in an operating state;

(2) measuring a flow rate of data of said selected device in said operating state;

(3) defining a predetermined flow rate of said selected device according to said flow rate of data measured in said step (2) to indicate said selected device is in a busy state;

repeating said steps (1)~(3) to define the predetermined flow rates of said devices fabricated on said motherboard;

measuring actual data flow rates of said devices on said motherboard;

when said actual data flow rate of one said device exceeds said predetermined flow rate thereof, promoting an operating rate of said device; and

when said actual data flow rate of said device is less than said predetermined flow rate thereof, reducing the operating rate of said device.

11. The method according the Claim 10, wherein said flow rate of data is the number of times of accessing data passing through said device per unit time.

12. The method according the Claim 10, wherein said flow rate of data is the number of times of transferring commands through said device per unit time.

13. The method according the Claim 10, wherein said devices on said motherboard comprise a CPU, a north bridge chip, a south bridge chip, an AGP slot, a PCI slot and a motherboard power supply.